SEMICONDUCTOR PACKAGE AND PACKAGE STACK MADE THEREOF

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This U.S. non-provisional application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 2002-74752 filed November 28, 2002, the entire contents of which are incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a semiconductor package and a package stack made thereof.

Description of the Prior Art

[0003] The electronic industry continues to seek products that are lighter, faster, smaller, multi-functional, more reliable and more cost-effective. In order to meet the requirement of the electronic industry, circuit chips should be more highly integrated.

[0004] However, increasing the density of integration of chips may be expensive and have technical limitations. Therefore, three-dimensional (3-D) type semiconductor packaging techniques have been developed and used. In general, package stacks made by stacking a plurality of packages and stacked chip packages made by stacking a plurality of chips in a package have been used.

[0005] Package stacks may be manufactured by stacking packages that have already passed the necessary tests for their functions. Therefore, the yields and reliability of

these package stacks may be higher than those stacked chip packages manufactured by stacking a plurality of chips without being tested. However, the package stacks may be thicker as compared with stacked chip packages, because of the thickness of each individual stacked package.

SUMMARY OF THE INVENTION

[0006] Exemplary embodiments of the invention provide a thinner semiconductor package, and a package stack using the thinner semiconductor package.

[0007] Exemplary embodiments of the invention also provide a semiconductor package, a package stack, a method of manufacturing a semiconductor package, and a method of manufacturing a package stack where one or more ends of one or more bonding wires are bonded to pads, such as bonding pads and/or board pads, using wedge bonding.

[0008] Exemplary embodiments of the invention also provide a semiconductor package, a package stack, a method of manufacturing a semiconductor package, and a method of manufacturing a package stack where two or more of solder bump pads, solder bumps, and an encapsulation part are provided on the same side of a board. In other exemplary embodiments, there are one or more solder bump pads, solder bumps, and/or encapsulation parts. In other exemplary embodiments, the side of the board is a lower side.

[0009] Exemplary embodiments of the invention also provide a semiconductor package, a package stack, a method of manufacturing a semiconductor package, and a method of manufacturing a package stack where two or more of solder bump pads, solder bumps, and an encapsulation part are provided on the same side of a board and where one or more ends of one or more bonding wires are bonded to pads, such as bonding pads and/or board pads, using wedge bonding.

[0010] An exemplary embodiment of the invention provides a semiconductor package comprising a board, a plurality of solder bump pads, a plurality of board pads, a plurality of wiring patterns, a plurality of contact pads, at least one chip, a plurality of bonding wires, an encapsulation part and a plurality of solder bumps.

[0011] The board may have an aperture, and the semiconductor chip may be installed in the aperture. The solder bump pads and the board pads may be formed on the lower surface of the board, and the solder bump pads may be electrically connected to board pads using the wiring patterns. The bonding pads may be formed on the semiconductor chip, and electrically connected to the board pads using the bonding wires. In order to reduce the height of loop of the bonding wires, both ends of the bonding wires may be attached to the bonding pads and the board pads by a wedge bonding.

[0012] The semiconductor chip, the bonding pads and the bonding wires may be encapsulated for protection. The contact pads may be formed on the upper surface of the board, and electrically connected to the solder bump pads by via holes.

[0013] The encapsulation part generally extends below the lower surface of the board. The height of each solder bump may be greater than the distance that the encapsulation part extend below the lower surface of the board.

[0014] The board may be covered with a solder resist except for the regions over the solder bump pads, the contact pads and the board pads.

[0015] A package stack according to an exemplary embodiment of the invention may be made by stacking the packages described above.

[0016] In the package stack according to an exemplary embodiment of the invention, the solder bumps of an upper package of any two adjacent packages may be electrically connected to the contact pads of the lower package of the two adjacent packages respectively.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. 1 is a perspective view of a semiconductor package according to an exemplary embodiment of the invention.

[0018] FIG. 2 is an enlarged view of the encircled part A in FIG. 1

[0019] FIG. 3 is a cross-sectional view of the cross section taken along 3-3 in FIG. 1.

[0020] FIG. 4 is a cross-sectional view of a package stack made of a plurality of the semiconductor packages according to an exemplary embodiment of the invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0021] Exemplary embodiments of the invention will be described below with reference to the accompanying drawings.

[0022] The structure of a semiconductor package (100) according to an exemplary embodiment of the invention will be described referring to FIG. 1 ~ FIG. 3. In FIG. 1 and FIG. 2, an encapsulation part (50) shown in FIG. 3 is not shown for convenience of explanation.

[0023] Referring to FIG. 1~FIG. 3, a semiconductor package according to an exemplary embodiment of the invention comprises a semiconductor chip (30), a board (10) and an electrical connector between the chip (30) and the board (10).

[0024] More specifically, the board (10) may comprise an upper surface (17), a lower surface (15) and an aperture (13) formed in a central region of the board (10). In FIG. 1, the package (100) is illustrated with the lower surface (15) of the board (10) upward.

[0025] In other exemplary embodiments, the board (10) may contain more than one aperture (13) and the aperture or apertures (13) may be located anywhere in the board (10).

[0026] The board (10) may be a printed circuit board having a body (12) and wiring patterns (14) formed on the body (12). The body (12) of the board (10) may be manufactured by using materials such as glass-epoxy resin or BT resin. The wiring patterns (14) may be formed by attaching thin copper foil on the board (10) , then patterning the copper foil.

[0027] A plurality of solder bump pads (26) may be formed on the lower surface (15) of the board (10) and electrically connected to the outer ends of the wiring patterns (14). A plurality of board pads (24) may be formed on the lower surface (15) of the board (10) near the aperture (13), and electrically connected to the other ends of the wiring patterns (14). Therefore, the board pads (24) may be electrically connected to the solder bump pads (26) one-to-one.

[0028] A plurality of contact pads (28) may be formed on the upper surface (17) of the board (10), and electrically connected to the solder bump pads (26) one-to-one by via holes (16) formed through the board (10). The via holes (16) may be made by making holes through the body (12) of the board (10), plating the inside surfaces of the holes with conductive materials such as Cu, then filling the holes with a low temperature melting metal such as solder.

[0029] Solder resist layers (18) may be formed on the upper surface (17) and the lower surface (15) of the body (12) in order to protect the body (12) and the wiring patterns (14). However, the solder resister layers (18) need not cover the areas over the aperture (13), the solder bump pads (26), the contact pads (28) and the board pads (24). The solder resist layer (18) formed on the lower surface (15) may play a role of preventing the liquid molding resins such as Epoxy Molding Compound (EMC) from flowing over the lower surface (15) of the board (10) during the molding process.

[0030] A plurality of bonding pads (34) may be formed on the active surface of semiconductor chip (30). The semiconductor chip (30) may be disposed in the

aperture (13) in the board (10) in such a manner that the active surface of the semiconductor chip (30) faces the same direction as the lower surface (15) of the board (10). The bonding pads (34) may be electrically connected to the board pads (24) by bonding wires (40). Each of the bonding wires has one end connected to one of the bonding pads (34) and the other end connected to one of the board pads (24) respectively by wedge bonding. Metals such as Au, Al or Cu may be used for making the bonding wires (40). By using wedge bonding at both ends of each bonding wire, it may be possible to control the maximum height of the loop of each bonding wire (40) within 0.05 mm. Using the conventional ball bonding method, it may be very difficult to control the maximum height of the loop of each bonding wire (40) within 0.05mm. In general, the wedge bonding may be carried out by an ultrasonic wedge bonding process or a thermosonic wedge bonding process. The ultrasonic wedge bonding process is a low temperature process (typically at ambient temperature) in which the welding is accomplished by force and ultrasonic energy. The thermosonic wedge bonding process is basically identical to the ultrasonic wedge bonding process, except for the additional step of component heating.

[0031] An encapsulation part (50) may be formed by filling the aperture (13) with a liquid molding resin, such as EMC. The liquid molding resin filling the aperture (13) becomes the encapsulation part (50) after it is cooled. The semiconductor chip (30), the bonding wires (40) and the board pads (24) are protected by the encapsulation part (50). The solder resist layer (18) formed on the lower surface (15) of the board (10) may prevent the liquid resin from flowing over entire area of the lower surface (15) of the board (10).

[0032] During the semiconductor chip installation process and the encapsulation process, adhesive tape may be attached to the upper surface (17) of the board (10), thereby closing the aperture (13) on the upper surface (17) of the board (10). During

the manufacturing process, the semiconductor chip (30) may be supported by the adhesive tape. The adhesive tape may be removed from the board (10) after the encapsulation process is finished. The inactive surface of the semiconductor chip (30) may be exposed to outside of the semiconductor package (100) in order to reduce the thickness of the package and to enhance the cooling effect of the semiconductor chip (30).

[0033] A plurality of solder bumps (60) are formed on the solder bump pads (26) respectively. In general, the solder bumps (60) may be made by reflowing the solders disposed on the solder bump pads (26).

[0034] According to an exemplary embodiment of the invention, the solder bumps (60) may be formed on the lower side of the board (10) in order to reduce the thickness of the package (100), because the encapsulation part (50) generally extends out of the board (10).

[0035] It may be possible to make the thickness (t1) of the board (10) less than 0.12 mm, and to make the thickness (t2) of the solder bump (60) less than 0.08 mm. Therefore, it may also be possible to make the total thickness (t) of the package (100) less than 0.2 mm.

[0036] By stacking the packages (100) according to an exemplary embodiment of the invention, it may be possible to obtain a thinner package stack. FIG. 4 is a cross sectional view of an exemplary embodiment of the invention showing a package stack made by stacking the packages (100).

[0037] According to FIG. 4, the package stack (200) is made by stacking five packages (100) 3-dimensionally. The solder bumps (60) of the upper package of any two adjacent packages are electrically connected to the contact pads (28) of the lower package of the two adjacent packages by reflowing the solder bumps. The solder bumps (60a) of the lowest package (100a) are generally used for outer terminals. In

order to stack the packages 3-dimensionally, the solder bump pads (26) of the upper package of any two adjacent packages may be aligned with the contact pads (28) of the lower package.

[0038] Because the thickness of each package (100) including the solder bumps may be less than 0.2mm, it may be possible to make the thickness of the package stack (200) less than 1.0 mm. Although an exemplary embodiment of the invention has been described with reference to five stacked packages, it is obvious to those of ordinary skill that the number of packages is not so restricted.

[0039] According to exemplary embodiments of the invention, it may be possible to obtain a thinner semiconductor package by connecting the semiconductor chip to the board using the wedge bonding method, and by forming the solder bumps on the lower side of the board where the encapsulation part is formed.

[0040] While the present invention has been particularly shown and described with reference to certain exemplary embodiments, it should be understood by those skill in the art that the scope of the present invention is defined by the claims provided below and is not restricted to the exemplary embodiments, and that various changes in form and details may be made without departing from the spirit and the scope of the invention.